REMARKS

Entry of this Amendment and reconsideration are respectfully requested in view of the amendments made to the claims and for the remarks made herein.

Claims 3-9 and 11-23 are pending and stand rejected. Claims 22 and 23 are objected to but would be allowable if rewritten in independent form.

Applicant thanks the Examiner for the indication of allowable subject matter in claims 22 and 23. However, for the arguments provided herein, applicant believes that the invention claimed in the instant application is not rendered obvious in view of the references cited.

More specifically, applicant notes that the instant application, filed January 23, 2002, claims priority to that patent application filed in the European Patent Office on January 23, 2001. Pursuant to MPEP 706.02(B)-(C), the effective date of the instant application is January 23, 2001, as the specification and claims of the instant application are essentially identical to those of the application filed in the European Patent Office.

With regard to the Vishakhadatta reference (USPub no. 2002/0141511) (serial no. 09/821,340), which is the primary reference cited against each of the claims, this application claims the benefit of the earlier filing date of Provisional patent application serial no. 60/273,119 filed on March 2, 2001, which further claims priority to Provisional patent Application serial no. 60/261,506, filed January 12, 2001.

With regard to determining the effective filing date of an application claiming the benefit of the filing date of a provisional patent application, "the effective filing date is the filing date of the provisional application for any claims which are fully supported under the first paragraph of 35 USC 112 by the provisional application." (see MPEP section 706.02(D)). ("The specification shall contain a written description of the invention and of the manner and process of making and using it, in such full, clear, concise and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention." 35 USC 112, first paragraph.

A review of the provisional patent applications reveals that the provisional application serial no. 60/273,119 includes 67 pages of specification and 19 pages of

drawings. However, with regard to provisional patent application serial no. 60/261,506, this provisional application contains 3 pages of specification and 1 page of drawings. A copy of the '506 provisional application is provided herein.

A review of the 60/261,506 provisional application shows a feature description of an integrated transceiver for wireless communications. The description generally describes the receiver and the transmitter operations of this product.

Applicant believes that based on a review of the material presented in the '506 provisional application and the difference between '506 and the '119 provisional applications and the filed 09/821,340 application, the '506 provisional application fails to fully support, as required by the first paragraph of 35 USC 112, the device claimed in the '340 application.

Applicant submits that the effective filing date of the Vishakhadatta reference is no earlier than March 2, 2001, which is latter than the effective filing date of the instant invention. Hence, the Vishakhadatta reference is not prior art which may be used to reject the claims of the instant invention.

For at least this reason, applicant submits that because each of the claims were rejected based on the Vishakhadatta reference, which has an effective filing date later than the instant invention, the rejection of the claims in the instant invention is improper. Hence, each of the claims is allowable over the cited references.

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For all the foregoing reasons, it is respectfully submitted that all the present claims are patentable in view of the cited references. A Notice of Allowance is respectfully requested.

Respectfully submitted,

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Date: August 31, 2006

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PROVISIONAL APPLICATION COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION under 37 CFR 1.53 (b)(2)

Docket Number	SILA:072PZ1	Type a plus sign (+) inside this box →	+

INVENTOR(s)/APPLICANT(s)

LAST NAME	FIRST NAME	MIDDLE INITIAL	RESIDENCE (CITY AND EITHER STATE OR FOREIGN COUNTRY)
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Tuttle	Tyson	G.	Austin, Texas
Srinivasan	Vishnu		Austin, Texas
Rafi	Aslam		Austin, Texas

TITLE OF THE INVENTION (280 characters max)

INTEGRATED TRANSCEIVER

CORRESPONDENCE ADDRESS

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ENCLOSED APPLICATION PARTS (*check all that apply*)

X Specification — *Number of Pages* 3 — X Small Entity

X Drawing(s) — *Number of Sheets* 1 — X Other (specify) postcard

METHOD OF PAYMENT (*check one*)

XA check or money order is enclosed to cover the Provisional filing fees X The Commissioner is hereby authorized to charge any credits or deficient fees to Deposit Account Number: 10-1205/ SILA:072PZ1	PROVISIONAL FILING FEE AMOUNT	$ 75

The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

X No.
____ Yes, the name of the U.S. Government agency and the Government contract number are:

Respectfully submitted,

SIGNATURE  Date January 12, 2001

NAME: REGISTRATION NO. Brian W. Peterman, Reg. 37,908 ☐

☐ Additional inventors are being named on separately numbered sheets attached hereto.

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I hereby certify that this paper or fee is being deposited with the United States Postal Service "EXRESS MAIL POST OFFICE TO ADDRESSEE" service under 37 C.F.R. 1.10 on the date indicated above and addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231


Signature

PROVISIONAL APPLICATION FILING ONLY

Si4200 / Si4201 Integrated Transceiver for GSM900, DCS1800 and PCS1900 Wireless Communications

Features

- Low-IF Receiver:
  - Dual or Triple-Band LNA
  - Image-Reject Down-Converter
  - High Performance A/D Converter
- Digital IF to Baseband Converter:
  - Down-Converter to Baseband
  - Channel-Select Filter
  - Gain Control
  - Universal Analog Interface
- Offset-PLL Transmitter:
  - High Precision I/Q Up-Converter
  - Integrated Transmit VCO
- GPRS Class 12 Compliant
- CMOS process technology
- 3-wire Serial Interface
- 2.7 to 3.3 V Operation

Applications

- Dual and Triple Band GSM Digital Cellular Handsets
- GPRS Wireless Data Modems

Description

The Si4200/Si4201 transceiver is designed to work with the Si4133T frequency synthesizer to form a complete RF front end for dual and triple band GSM digital cellular mobile station applications. The transmit section interfaces between the baseband processor and the power amplifier. The receive section interfaces between the antenna band-select SAW filters and the baseband processor. No external IF SAW filter or VCO modules are required as all functions are completely implemented on-chip.

Functional Description

General Description

The Si4200/Si4201 transceiver is designed to work with the Si4133T frequency synthesizer to form a complete RF front end for dual and triple band GSM digital cellular mobile station applications. The transmit section interfaces between the baseband processor and the power amplifier. The receive section interfaces between the antenna band-select SAW filters and the baseband processor. No external IF SAW filter or VCO modules are required as all functions are completely implemented on-chip.

Receiver

The receive (Rx) section converts the RF antenna signal from EGSM (925 to 960 MHz), DCS (1805 to 1880 MHz), and PCS (1930 to 1990 MHz) bands down to an analog baseband I/Q signal. The RF antenna signal is first passed through a switch and band-select SAW filters. Three differential-input LNAs are integrated (one for each band) and are matched to the SAW outputs through external matching networks. The LNA is followed by an image-reject downconverter, an analog programmable gain amplifier, A/D converters (ADCs), a digital I/Q baseband down-converter, a digital channel select filter, a digital programmable gain amplifier, and I/Q D/A converters (DACs).

The receive path gain is programmable with variable gain elements including the LNA, analog PGA, and digital PGA. The DACs have programmable full scale and common mode I/Q outputs, and are designed to drive the analog inputs on industry standard baseband processors.

The Si4201 contains a digital IIR filter for channel selection. The response of this filter may be programmed to a narrow bandwidth setting (CSEL=1) designed to give high selectivity of a single GSM channel, or to a wider bandwidth setting (CSEL=0) designed to reduce the signal dynamic range to levels supported by the DAC and associated ADC on a typical baseband chip. The wider bandwidth setting reduces the total group delay (latency) of the receiver, which may be desirable in architectures containing a final channelization filter in the baseband chip.

The Si4133T frequency synthesizer generates the RF local oscillator (RFLO) between 1804.9 and 1989.9 MHz. The RFLO is divided by 2 in GSM mode. The 100 kHz IF local oscillator (IFLO) for the I/Q down-converter is digitally synthesized from the crystal oscillator reference clock. The low IF architecture eases image rejection requirements, and allows for on-chip integration of the channel select filters.

Initialization of the receive path occurs upon power up (rising edge of PDNB). The initialization sequence is automatically executed.

Transmitter

The transmit (Tx) section consists of an I/Q baseband up-converter, an offset phase-locked loop (OPLL) and two output buffers that can drive external power amplifiers (PA), one for the GSM band and one shared between the DCS and PCS bands. The entire transmit path, including the transmit VCO, is fully integrated on the Si4200. The quadrature mixer up-converts the differential in-phase (TXIP, TXIN) and quadrature (TXQP, TXQN) signals with the IFLO to generate a SSB IF signal which is used as the reference input to the OPLL. The OPLL consists of two mixers, one low pass filter and one VCO. The transmit VCO is centered between the DCS and PCS bands, and its output is divided by two for the GSM band.

The OPLL architecture attenuates signals outside its bandwidth, acting like a bandpass filter. The bandwidth of the PLL is such that a reference signal that falls within the GSM spectral mask is reproduced at the output of the VCO. Any transmit noise or spurious tones that might exist in the reference signal outside the PLL bandwidth are attenuated, significantly reducing the requirement for filtering at the antenna, which in turn minimizes system cost, part count, insertion loss and power consumption. This is one of the advantages of using this structure over a direct upconversion architecture where an external duplexer is needed to attenuate transmitter noise in the receive band. Additionally, the output of the VCO is a constant-amplitude signal which reduces the problem of spectral spreading caused by non-linearity in the PA.

When transmitting, the Si4133T frequency synthesizer generates the RFLO and IFLO signals. High-side injection is utilized for the GSM band, and low-side injection for DCS and PCS, so that the RFLO frequency remains situated midway between the GSM and DCS/PCS bands for both modes of operation.

Initialization of the transmit path occurs upon power up (rising edge of PDNB). The initialization sequence is automatically executed.

Serial Interface

A three-wire serial interface is provided to allow an external system controller to write the control registers for dividers, receive path gain, power down settings, and other controls. The serial interface is intended to be connected in parallel to both the Si4201 and the Si4133T. Serial control is relayed from the Si4201 to the Si4200 over the signal interface (IOP/N and CKP/N pins). All registers must be written when PDNB is low (powered down). The single logical register space is allocated among the three chips.

The serial control word is 22 bits, comprised of a 16-bit data field and a 6-bit address field. When the serial interface is enabled (i.e., when SENB is low), data and address bits on the SDI pin are clocked into an internal shift register on the rising edge of SCLK. Data in the shift register is then transferred on the rising edge of SENB into the internal data register addressed in the address field. The serial interface is disabled when SENB is high. It is not necessary (although it is permissible) to clock into the internal shift register any leading bits that are "don't cares."

All of the serial interface pins should be held at a constant level during receive and transmit bursts in order to minimize spurious emissions. This includes stopping the SCLK clock.